

# DATA SHEET



## **PEMH4**

NPN resistor-equipped double  
transistor  $R1 = 10\text{ k}\Omega$ ,  $R2 = \text{open}$

Preliminary specification

2001 Sep 14

# NPN resistor-equipped double transistor

R1 = 10 kΩ, R2 = open

**PEMH4**

**FEATURES**

- 300 mW total power dissipation
- Very small 1.6 mm × 1.2 mm × 0.55 mm ultra thin package
- Excellent coplanarity due to straight leads
- Reduces number of components as replacement of two SC-75/SC-89 packaged transistors
- Reduces required board space
- Reduces pick and place costs.

**APPLICATIONS**

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit driver.

**DESCRIPTION**

NPN resistor-equipped double transistor in a SOT666 plastic package.

**MARKING**

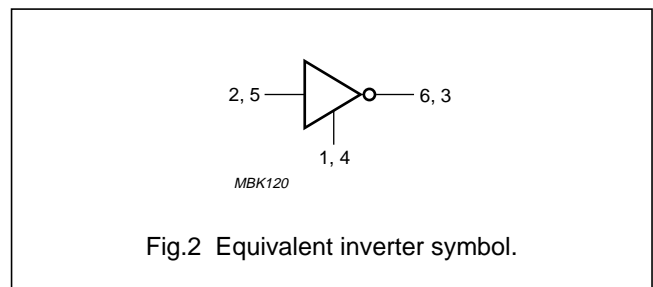
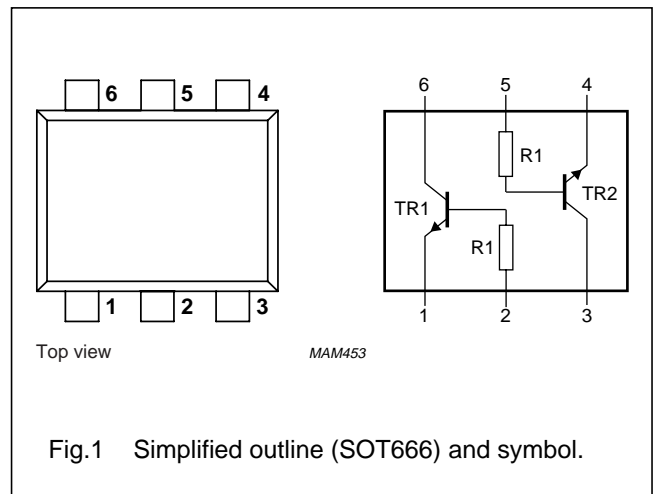
TYPE NUMBER	MARKING CODE
PEMH4	H4

**PINNING**

PIN	DESCRIPTION
1, 4	emitter TR1; TR2
2, 5	base TR1; TR2
6, 3	collector TR1; TR2

**QUICK REFERENCE DATA**

SYMBOL	PARAMETER	MAX.	UNIT
V <sub>CEO</sub>	collector-emitter voltage	50	V
I <sub>CM</sub>	peak collector current	100	mA
TR1	NPN	–	–
TR2	NPN	–	–
R1	bias resistor	10	kΩ



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**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
<b>Per transistor</b>					
V <sub>CBO</sub>	collector-base voltage	open emitter	–	50	V
V <sub>CEO</sub>	collector-emitter voltage	open base	–	50	V
V <sub>EBO</sub>	emitter-base voltage	open collector	–	5	V
I <sub>O</sub>	output current (DC)		–	100	mA
I <sub>CM</sub>	peak collector current		–	100	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C; note 1	–	200	mW
T <sub>stg</sub>	storage temperature		–65	+150	°C
T <sub>j</sub>	junction temperature		–	150	°C
T <sub>amb</sub>	operating ambient temperature		–65	+150	°C
<b>Per device</b>					
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C; note 1	–	300	mW

**Note**

1. Transistor mounted on an FR4 printed-circuit board.

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R <sub>th j-a</sub>	thermal resistance from junction to ambient	notes 1 and 2	416	K/W

**Notes**

1. Transistor mounted on an FR4 printed-circuit board.
2. The only recommended soldering method is reflow soldering.

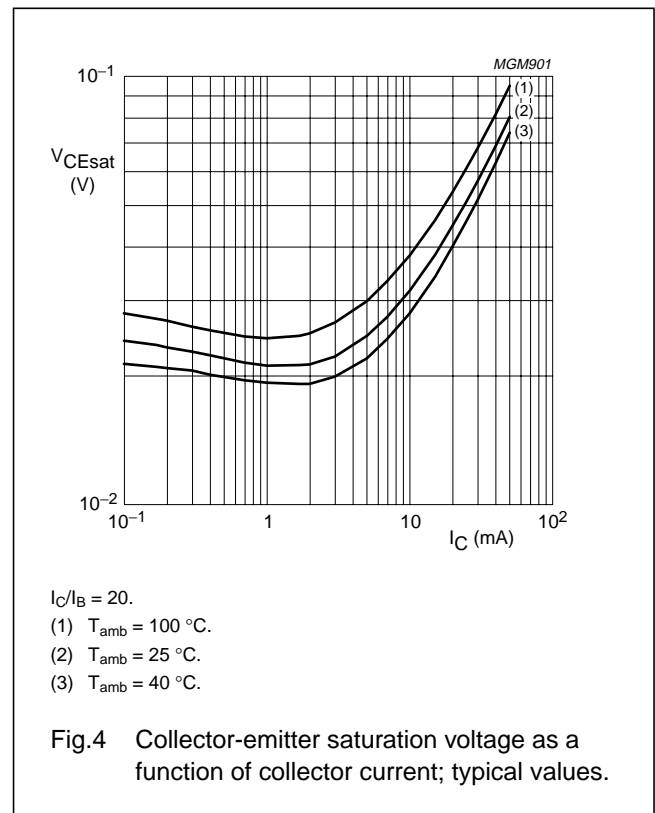
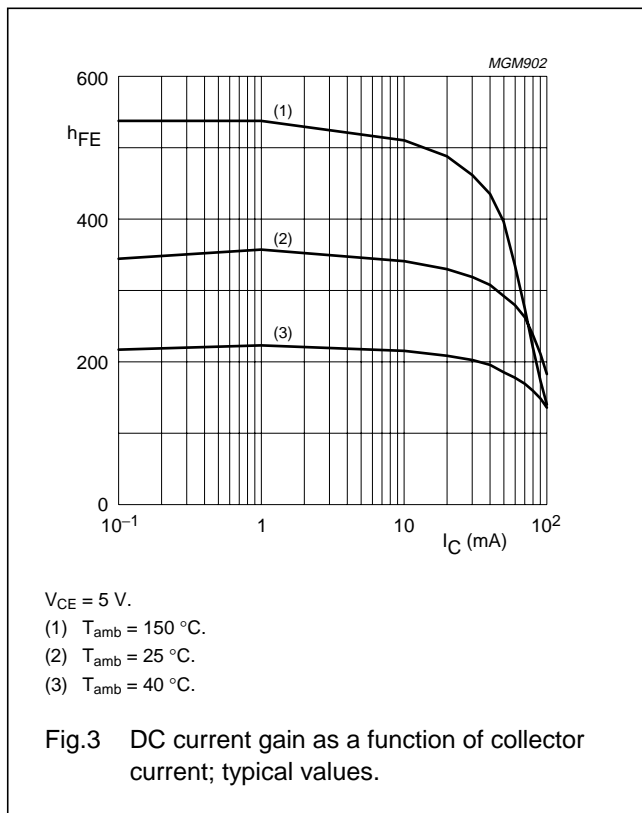
**NPN resistor-equipped double transistor**  
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**CHARACTERISTICS**

T<sub>amb</sub> = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Per transistor</b>						
I <sub>CBO</sub>	collector cut-off current	I <sub>E</sub> = 0; V <sub>CB</sub> = 50 V	–	–	100	nA
I <sub>CEO</sub>	collector cut-off current	I <sub>B</sub> = 0; V <sub>CE</sub> = 50 V	–	–	1	μA
		I <sub>B</sub> = 0; V <sub>CE</sub> = 30 V; T <sub>j</sub> = 150 °C	–	–	50	μA
I <sub>EBO</sub>	emitter cut-off current	I <sub>C</sub> = 0; V <sub>EB</sub> = 5 V	–	–	100	μA
h <sub>FE</sub>	DC current gain	I <sub>C</sub> = 1 mA; V <sub>CE</sub> = 5 V	200	–	–	
V <sub>CEsat</sub>	collector-emitter saturation voltage	I <sub>C</sub> = 5 mA; I <sub>B</sub> = 0.25 mA	–	–	150	mV
R1	input resistor		7	10	13	kΩ
C <sub>c</sub>	collector capacitance	I <sub>E</sub> = i <sub>e</sub> = 0; V <sub>CB</sub> = 10 V; f = 1 MHz	–	–	2.5	pF



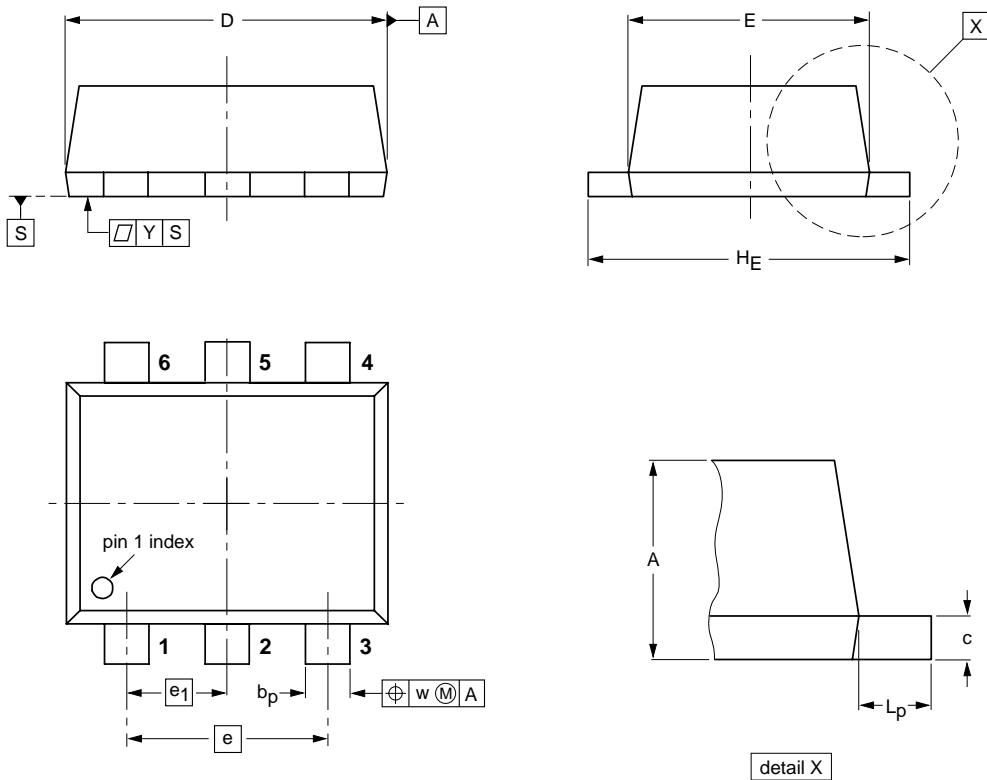
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PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT666



DIMENSIONS (mm are the original dimensions)

UNIT	A	$b_p$	c	D	E	e	$e_1$	$H_E$	$L_p$	w	y
mm	0.6 0.5	0.27 0.17	0.18 0.08	1.7 1.5	1.3 1.1	1.0	0.5	1.7 1.5	0.3 0.1	0.1	0.1

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT666					-01-01-04 01-08-27

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## DATA SHEET STATUS

DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITIONS
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**NOTES**

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